

# TC9192P/F

DOUBLE PLL FOR MOTOR CONTROL

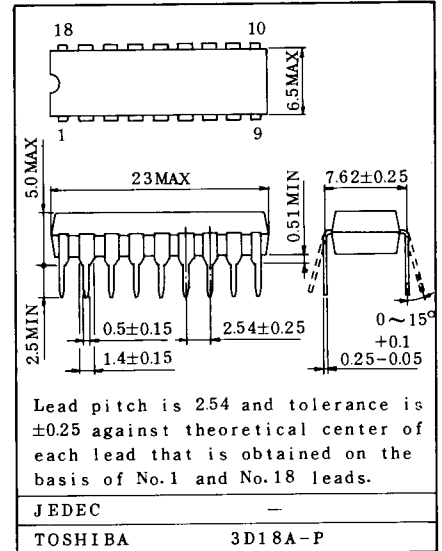
This is a LSI designed for motor-controlling the copying machine of which motor-rotation speed is necessary to be varied freely. With built-in PLL and VCO for reference signal generation, reference frequency can voluntarily be varied externally.

- Through using built-in VCO, PD, phase comparator and divider reference frequencies can be obtained.
- AFC and APC applied with 8-bit D/A converter system is incorporated, and transistor of bipolar type is provided at the output for Buffer Amplifier
- Lock range can be switched.
- Reference voltage output for filter-amplifier is provided.
- Lock detection output and reverse rotation signal output are provided.

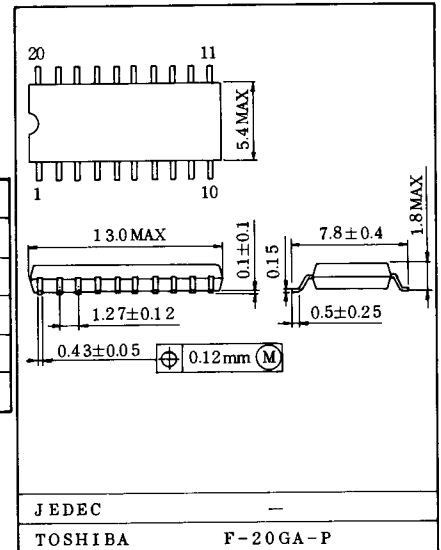
## MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V <sub>DD</sub>	-0.3~7.0	V
Input Voltage	V <sub>IN</sub>	-0.3~V <sub>DD</sub> +0.3	V
Power Dissipation	PD	300	mW
Operating Temperature	T <sub>opr</sub>	-30~75	°C
Storage Temperature	T <sub>stg</sub>	-55~125	°C

Unit in mm

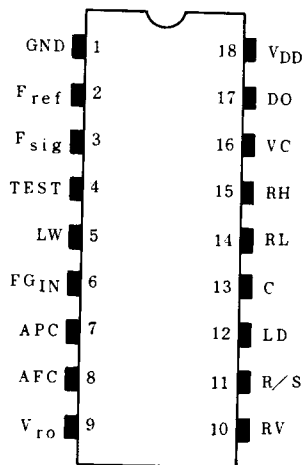


Unit in mm

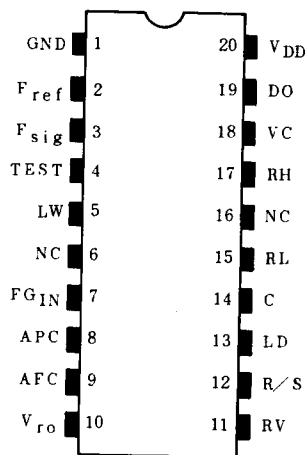


PIN CONNECT

TC9192P

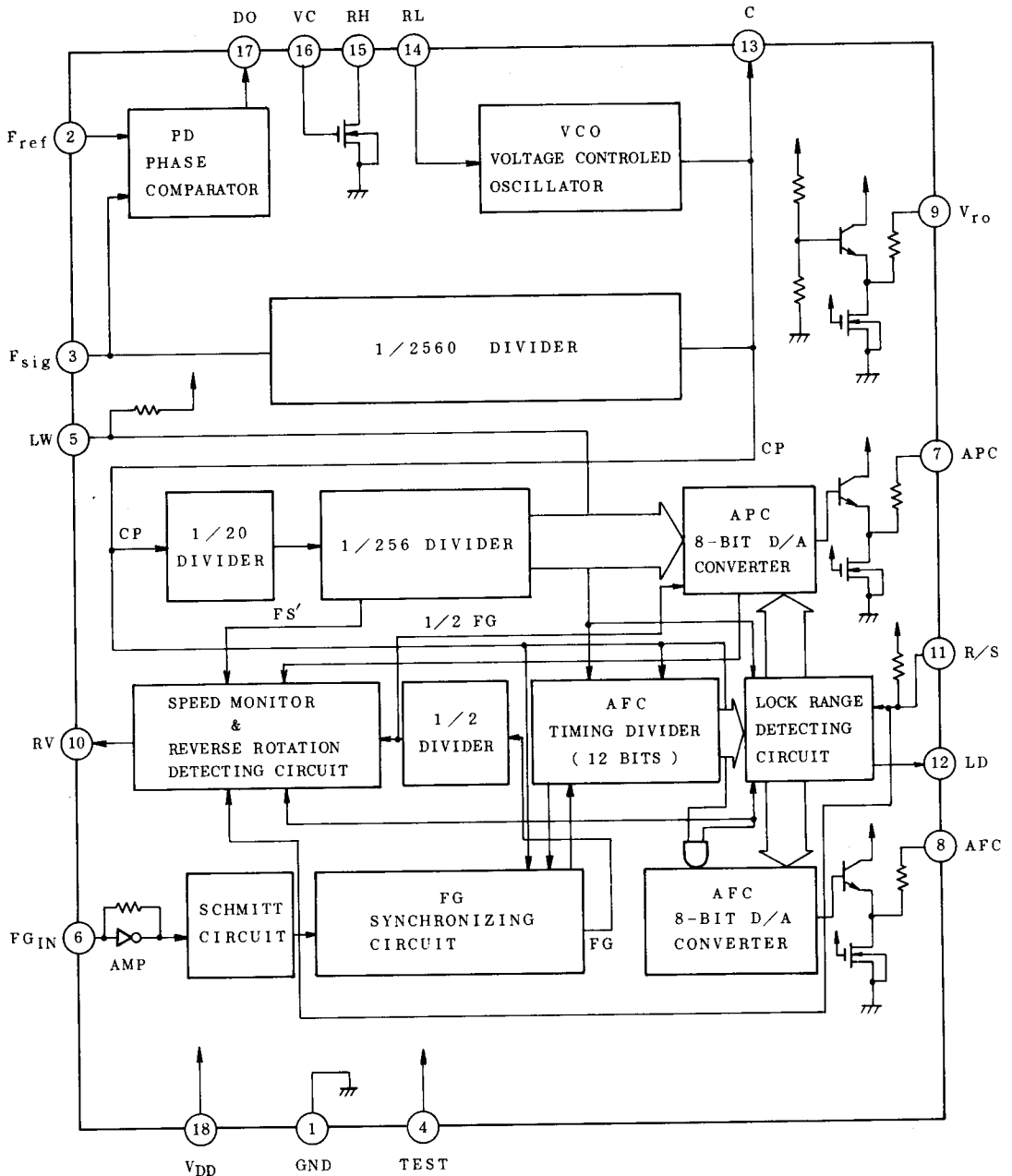


TC9192F

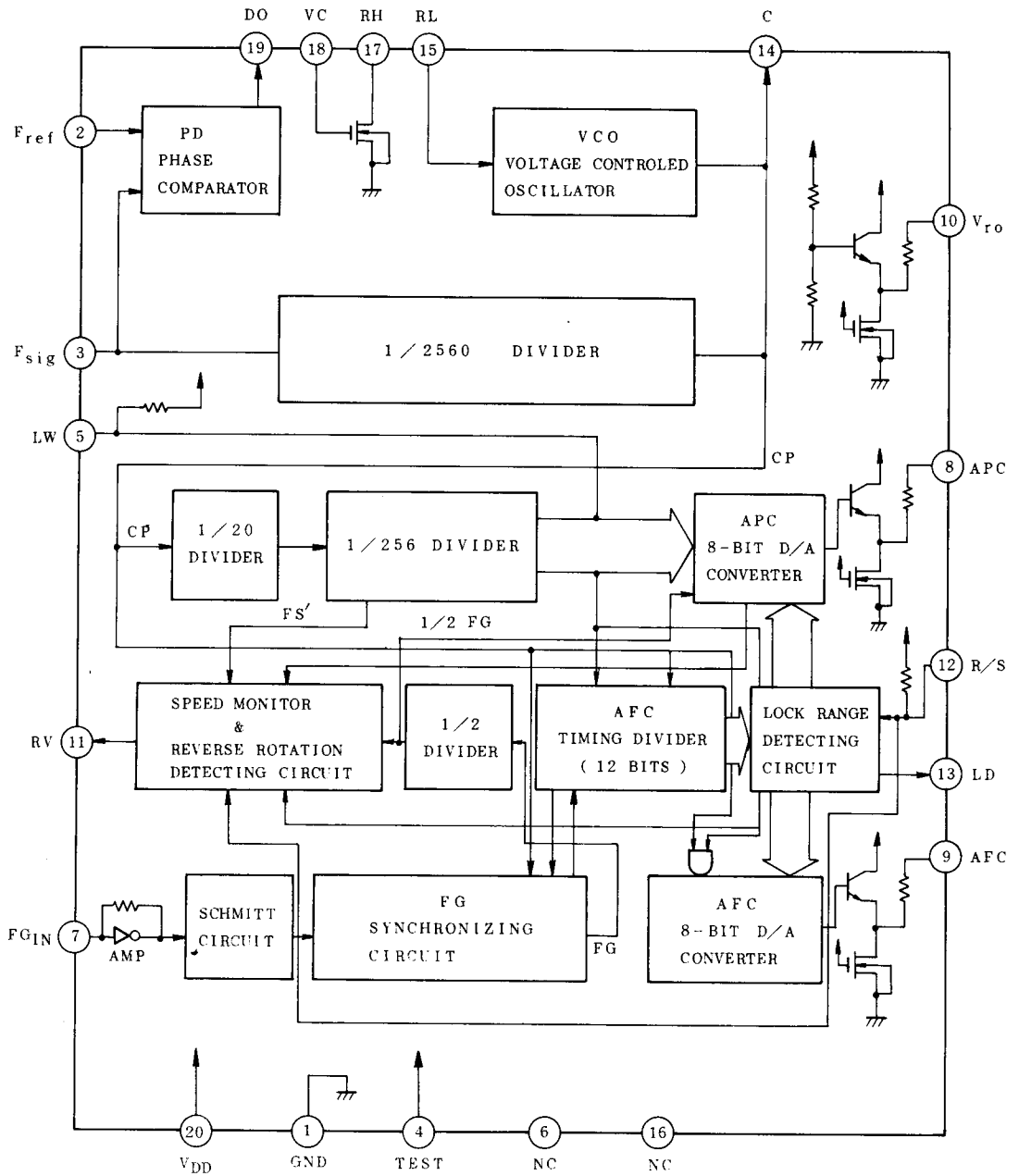


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BLOCK DIAGRAM TC9192P



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ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=25°C, VDD=5V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Power Supply Voltage	VDD		4.5	~	5.5	V
Power Supply Current	IDD	*	-	7	20	mA

## VCO BLOCK

Max. Operating Frequency	fVCO Max	C=33pF, RL=0V	*	4.0	6.0	-	MHz
VCO Applicable Range	fVCO	Constant of C is varied with fVCO	*	0.5	~	4.0	MHz
VCO Deviation	ΔfVCO	C=Constant, RL=2.0V	*	-	±50	-	%
VCO Fsig Frequency Range	fCPIN	Fsig N=2560	*	0.5	~	4.0	MHz

## FG AMPLIFIER BLOCK

Operating Frequency Range	fFG	VIN=0.5Vp-p	*	-	~	10	kHz
Input Operating Voltage	VFG	fFG=10kHz, Sine wave	*	0.5	~	VDD-0.5	Vp-p
Fref Frequency Range	fref		*	0.2	~	2.0	kHz

## APC, AFC, D/A CONVERTER BLOCK

Max. Deviation		Measuring at buffer output		-	±2.5	±6.5	LSB
Resolution				-	VDD/256	-	
Ladder Resistance	RD			30	50	70	kΩ

## BIPOLEAR TRANSFORMER OUTPUT CURRENT (APC, AFC, Vro TERMINAL)

Output Current	"H" Level	IOHB	VOH=3V	-	-1.6	-0.8	mA
	"L" Level	IOLB	VOL=2V	30	50	200	μA
Output Voltage		Vro	Reference Output Voltage	1.6	1.9	2.2	V

## PHASE COMPARATOR CHARACTERISTIC (DO TERMINAL)

Output Current	"H" Level	IOHDO		~	-	-1.0	mA
	"L" Level	IOLD0		1.0	2.0	~	
Output Leak Current at OFF		IOZDO		-	-	±0.1	μA
Input Leak Current		IIH/IIL	Fref, VC terminal	~	-	±1.0	μA
Pull-up Resistance		RIN	LW, R/S terminal	15	30	45	kΩ
Input Voltage	"H" Level	VIH	FGIN, LW, R/S terminal	0.7×VDD	~	VDD	V
	"L" Level	VIL	Fref	0	~	0.3×VDD	
Output Current	"H" Level	IOH	RV, LD terminal	VOH=4V	-	-1.0	mA
	"L" Level	IOL		VOL=1V	0.5	1.0	

## Nch OPEN DRAIN CURRENT

Nch ON Current	IOLD	RH terminal	VC=5V	1.5	2.5	-	mA
Nch OFF Current	IOID		VC=0V	-	-	±1.0	μA

\* : Guaranteed within the range of VDD=4.5V~5.5V, Ta=-30~75°C.

FUNCTIONAL DISCRIPTION OF EACH PIN

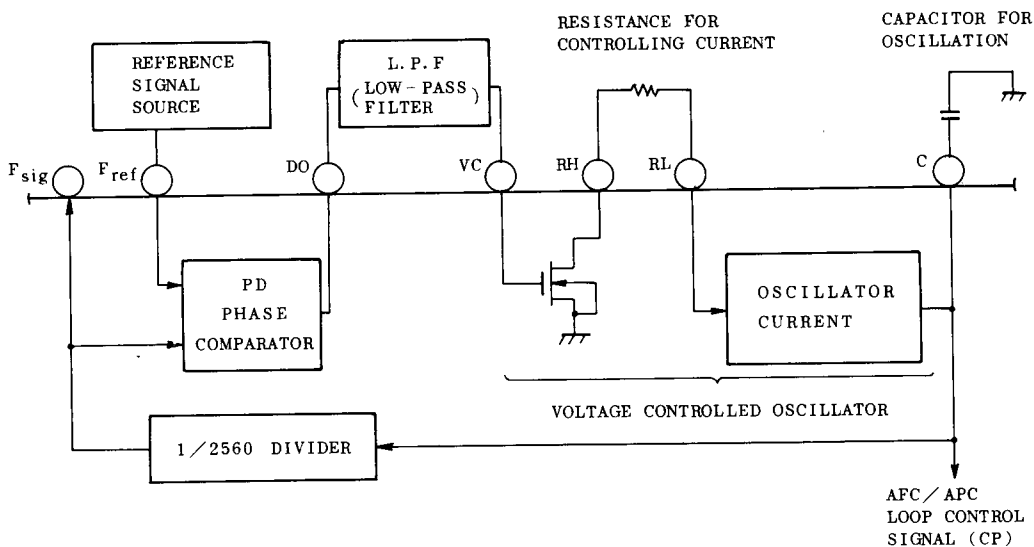
PIN No.		SYMBOL	FUNCTION, OPERATION	REMARKS
P	F			
18	20	VDD	Power supply voltage terminal and grounding terminal.	
1	1	GND		
2	2	F <sub>ref</sub>	Reference frequency input terminal for phase comparator.	C-MOS input
3	3	F <sub>sig</sub>	1/2560 dividing output terminal of VCO frequency, internally comparison signal is made.	C-MOS output
5	5	LW	Switching terminal of lock range. at LW="H", normal range. at LW="L", double range.	Built-in pull-up resistance speed
6	7	FGIN	Pulse input terminal for indicating the rotation speed of motor.	Built-in amp.
7	8	APC	Output terminal of APC 8-bit D/A converter output.	Built-in bipolar transistor
8	9	AFC	Output terminal of AFC 8-bit D/A converter output.	Built-in bipolar transistor
9	10	V <sub>ro</sub>	Output terminal for reference voltage.	Built-in bipolar transistor
10	11	RV	Reverse rotation signal for output driver.	C-MOS output
11	12	R/S	RUN/STOP switching terminal of motor at R/S="L", RUN. at R/S="H", STOP	Built-in pull-up resistance
12	13	LD	Lock detecting terminal. When the rotation frequency is within lock range, "H" level, and in other cases, "L" level.	C-MOS output
13	14	C	Terminal attached with capacitor for adjusting frequency. Internal control signal is made.	
14	15	RL	Current control terminal for controlling VCO frequency.	
15	17	RH	Current control output terminal for VCO	
16	18	VC	Voltage control input terminal for VCO	
17	19	DO	Output terminal of phase comparator	C-MOS input
4	4	Tset	Input terminal of internal test. Generally ground.	C-MOS input
-	6,16	NC	No connect	

# TC9192P/F

## EXPLANATION OF OPERATION

TC9192P/F has double PLL which is consist of AFC/APC loop for motor-controlling and phase feedback loop for reference signal. In the following operation of respective block is explained.

### 1. Phase Feedback Loop



#### (1) Voltage controlled oscillator terminal (C,RL,RH,VC)

. Voltage controlled oscillator (VCO) is consist of the Nch open drain FET (VC,RH, terminal) and current controlled oscillator (RL,C terminal) combined.

VCO is an oscillator of which oscillation frequency is controlled by given control voltage. The control voltage and oscillation frequency are proportional.

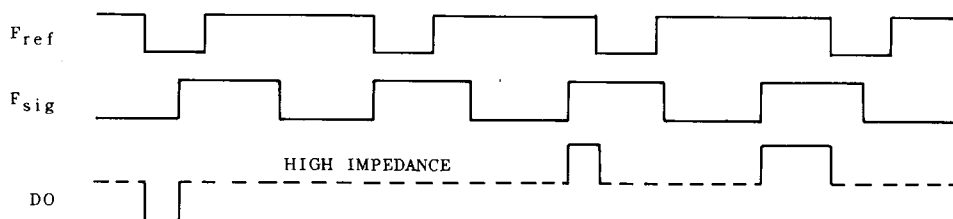
. The operation frequency range of VCO is 0.5~4MHz.

. Frequency which is obtained by VCO becomes control signal (CP) of AFC, APC loop in next step.

(2) Phase comparator output terminal (Fsig, Fref, DO)

- . Phase comparator detects the input pulse difference, and outputs at DO the positive and the negative pulses proportioned with the phase difference.

PHASE COMPARATOR TIMING CHART



- . Fref terminal is reference signal input terminal of APC/AFC loop control signal (CP), the motor speed (the number of FG pulses of motor) is decided by it.

The relations between FG, Fref and FG is as follows;

$$f_x(\text{CP}) = 2560 \times F_{\text{ref}}[\text{Hz}] : \text{Relation between } F_{\text{ref}} \text{ and control signal (CP)}$$

$$f_x(\text{CP}) = 20 \times 128 \times \text{FG}[\text{Hz}] : \text{Relation between FG and control signal (CP)}$$

∴ This relation becomes "FG=Fref[Hz]"

- . Fref input terminal is a C-MOS structure.
- . Fsig output terminal is output comparison signal of phase comparator.

2. APC/AFC Loop

(1) FG pulse input terminal (FGIN)

- . This is the input terminal of FG pulse for indicating the motor speed, and this signal becomes the comparison frequency of internal PLL.
- . Since the amplifier and the Schmitt circuit are incorporated, operation is made with the small amplitude through the coupling capacitor.



## TC9192P/F

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(2) Output terminals (APC, AFC) of phase control system (APC) and speed control system.

. AFC is F-V converter against  $FG_{IN}$  frequency and is fabricated with 8-bit D/A converter.

. APC is the phase comparator ( $\phi$ -V converter) for comparing the phase difference  $\phi$  between  $\frac{1}{2}FG$  signal and the reference signal  $FS'$ , and is also fabricated with 8-bit D/A converter.

(Note)  $FS' = \frac{1}{2} FS$

. Both APC and AFC perform three kinds of operations described below.

a) When  $FG_{IN}$  frequency is within the lock range, both APC and AFC perform the normal operation against  $FG_{IN}$ .

Against the reference synchronization  $FS$ , the lock range is

at  $LW="L"$ , +9.3%, -10.6% (about  $\pm 10\%$ )

at  $LW="H"$ , +4.6%, -5.3% (about  $\pm 5\%$ )

(Note) Reference frequency  $FS = \frac{f_x(CP)}{20 \times 128}$  [Hz]

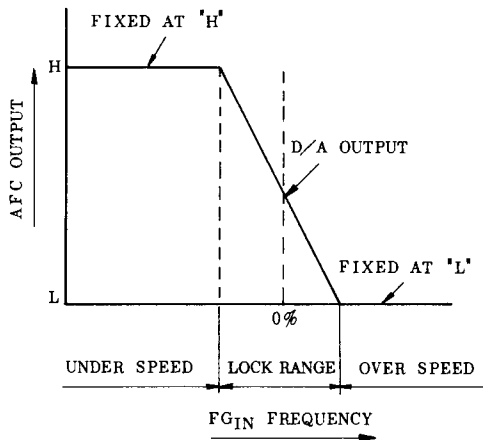
b) When  $FG_{IN}$  frequency is under the lock range (under speed), the outputs of APC and AFC are fixed at "H" level.

c) When  $FG_{IN}$  frequency is over the lock range (over speed), the outputs of APC and AFC are fixed at "L" level.

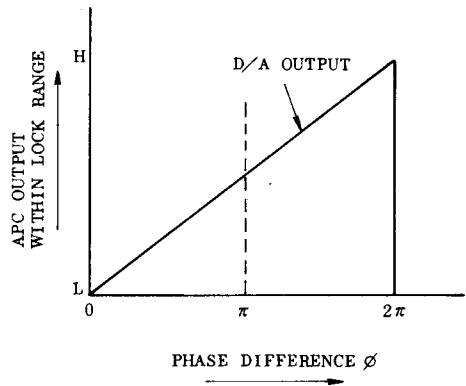
. When the motor is in STOP state ( $R/S=H$  or Open), both the outputs of AFC and APC are fixed at "L" level.

. Bipolar transformer is incorporated at the output stage of both APC and AFC.

CHANGE OF APC OUTPUT AGAINST  $FG_{IN}$  FREQUENCY

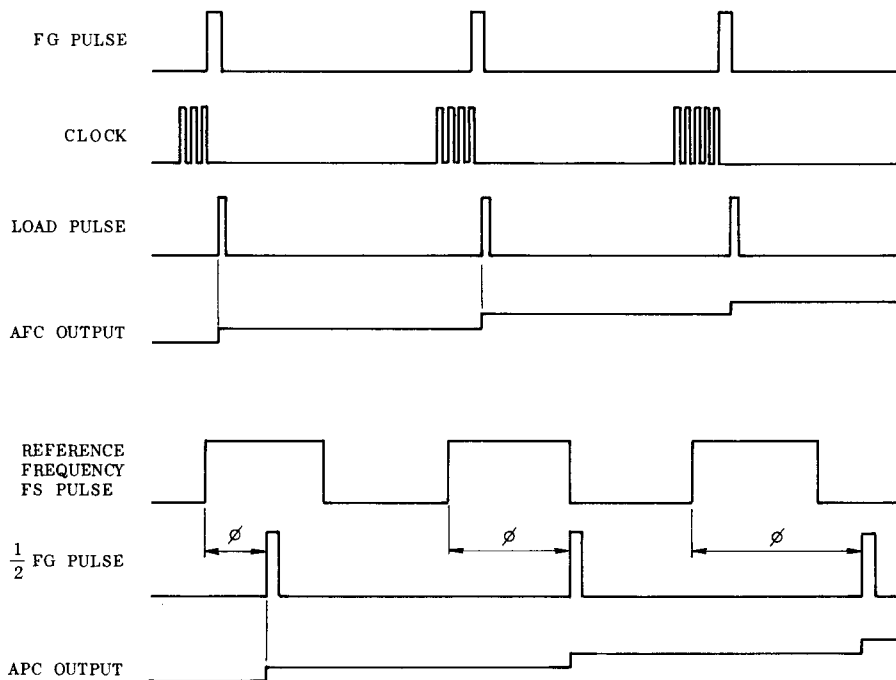


CHANGE OF APC OUTPUT AGAINST PHASE DIFFERENCE  $\phi$



. Timing charts of AFC and APC within lock range

a. AFC (speed control system)



(3) Output terminal for reference voltage generation ( $V_{ro}$ )

- .  $V_{ro}$  is the transistor output terminal for the reference voltage of the operational amplifier which controls the motor by means of synthesizing the outputs of APC and AFC.
- .  $V_{ro}$  is fixed at  $\frac{1}{2} V_{DD} - V_F$  internally through dividing the resistance, and the output is fabricated into bipolar transistor construction.

(4) Lock range switching input terminal (LW)

- . This is the terminal for switching the lock range of APC and AFC, and two kinds of lock ranges can be selected through operating this terminal.
  - at LW="H", normal lock range ( $\pm 5\%$ )
  - at LW="L", double lock range ( $\pm 10\%$ )

(5) RUN/STOP input terminal (R/S)

- . RUN/STOP signals of motor are input. RUN="L", STOP="H" or open
- . During RUN(R/S=L), APC, AFC and LD perform the normal operation against  $FG_{IN}$  frequency. During STOP(R/S=H or Open), APC, AFC and LD are all fixed at "L" level.
- . Pull-up resistance and chattering prevention circuit are incorporated.

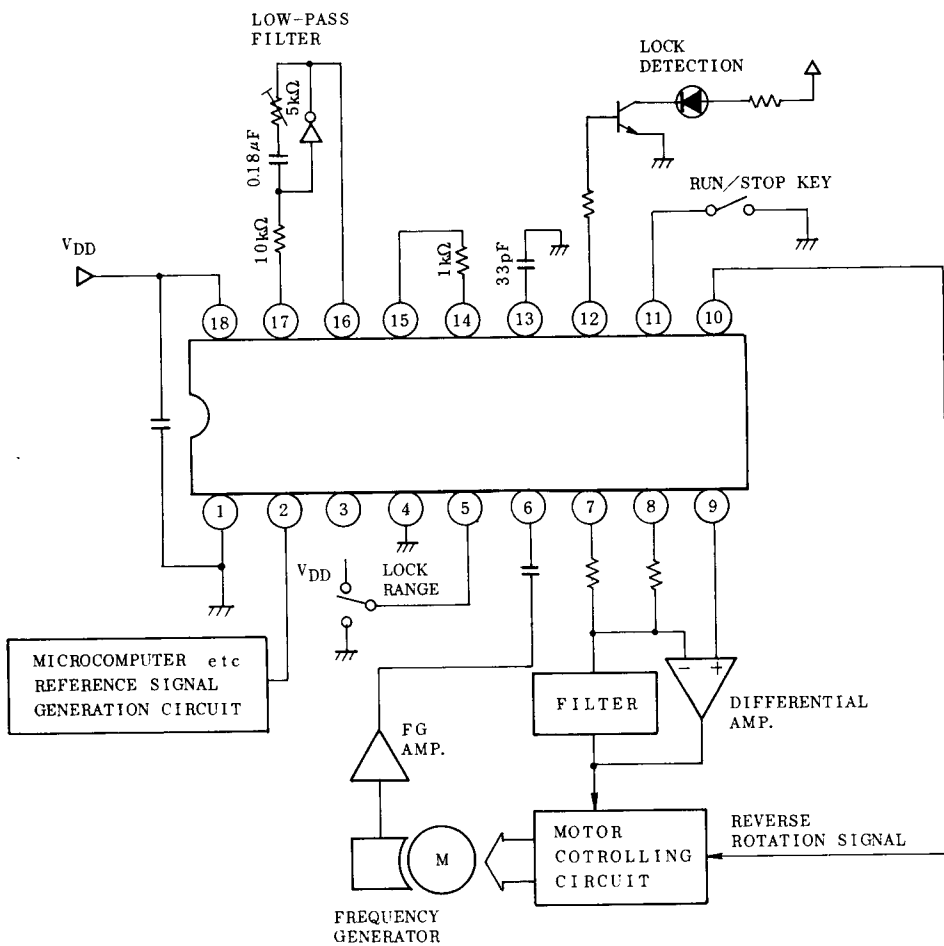
(6) Lock detection terminal (LD)

This is the output terminal for lock detection. When  $FG_{IN}$  frequency is within lock range, the terminal is at "H" level, and in other cases, at "L" level.

(7) Reverse rotation signal output terminal (RV)

- . RV is the reverse rotation signal output for applying the brake to the motor when the motor is changed to STOP state.
- . When STOP state is turned out, RV becomes "H" level, and when the frequency of  $FG_{IN}$  becomes below  $\frac{1}{8} FS$ , "L" level. In other cases, RV is fixed at "L" level.

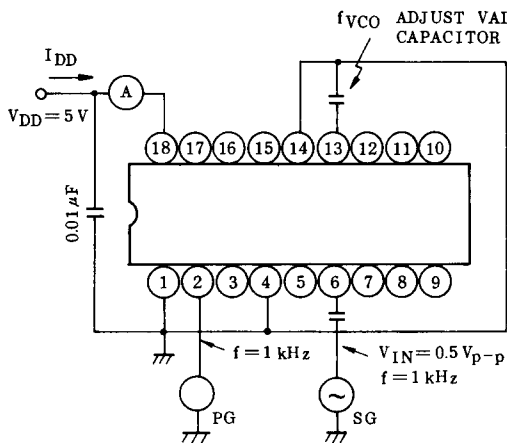
EXAMPLE OF APPLICATION CIRCUIT (Pin connect is TC9192P)



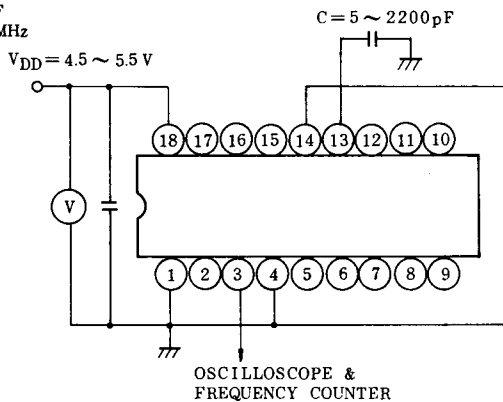
# TC9192P/F

CHARACTERISTIC TEST CIRCUIT (Pin connect is TC9192P)

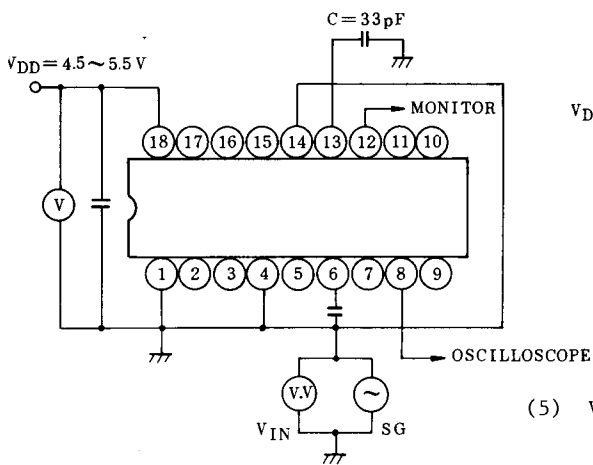
(1) Operating Supply Current ( $I_{DD}$ )



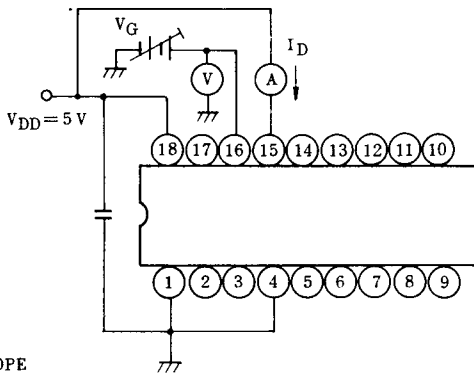
(2) VCO Operating Frequency Range ( $f_{VCO}$ )



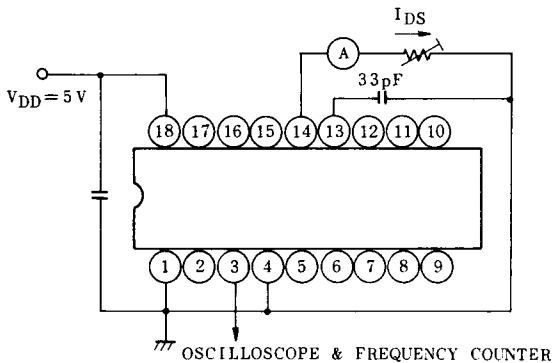
(3)  $FG_{IN}$  Input Sensitivity



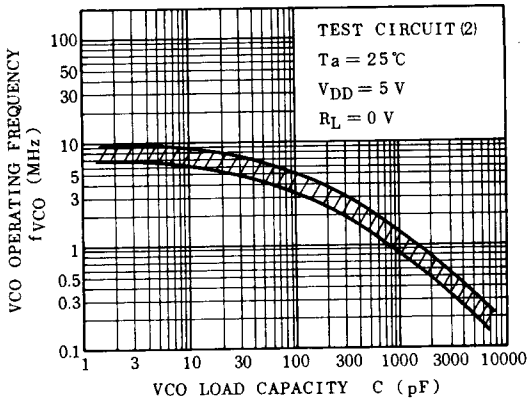
(4) Nch Open Drain Current ( $I_D$ )



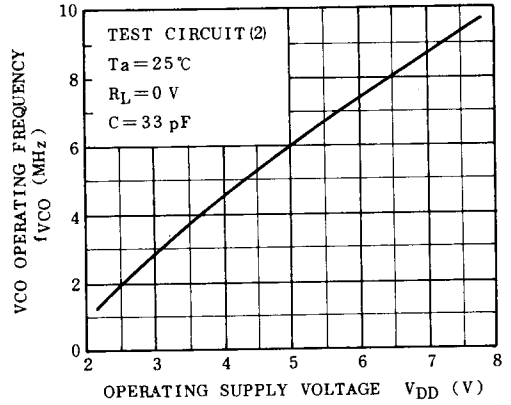
(5) VCO Operating Frequency Range (2) ( $f_{VCO}$ )



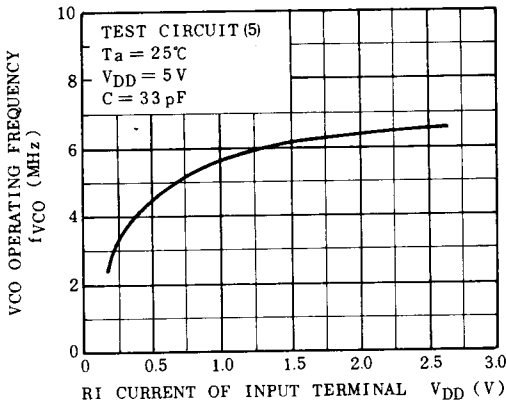
C - f<sub>VCO</sub>



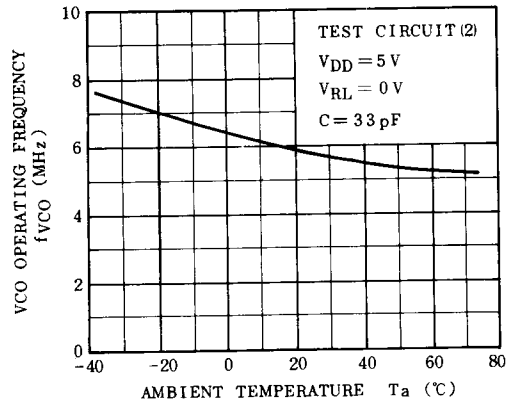
V<sub>DD</sub> - f<sub>VCO</sub>



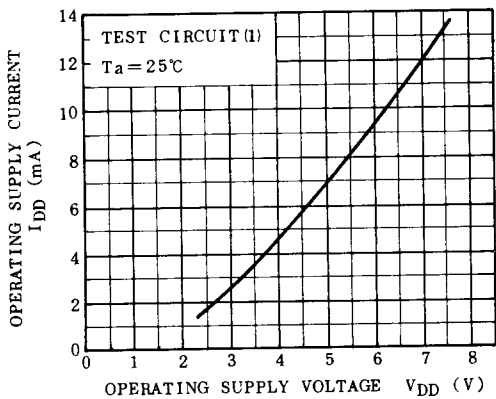
I<sub>DS</sub> - f<sub>VCO</sub>



T<sub>a</sub> - f<sub>VCO</sub>



V<sub>DD</sub> - I<sub>DD</sub>



V<sub>G</sub> - I<sub>D</sub>

